UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,929	11/06/2003	David A. Beeson	60702.300401	2928

32112 7590 11/18/2005

INTELLECTUAL PROPERTY LAW OFFICE
1901 S. BASCOM AVENUE, SUITE 660
CAMPBELL, CA 95008

EXAMINER	
AGHDAM, FRESHTEH N	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 11/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,929	BEESON ET AL.	
	Examiner	Art Unit	
	Freshteh N. Aghdam	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-18 and 21-27* is/are rejected.

7)☒ Claim(s) *5,6,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 8-9, and 16-18, 22- are rejected under 35 U.S.C. 103(a) as being unpatentable over Koudelka (US 6,859,509), and further in view of Hsu (US 2004/0008087).

As to claims 1 and 16, Koudelka teaches a rate detector for detecting the rate of the input data signal and providing a plurality of range signals specifying progressively high to low ranges encompassing the rate (Fig. 2, means 22 and 24; Col. 2, Lines 19-42); a phase detector (Fig. 9, means 80) for providing a phase error signal based on the input data signal and the recovered signal; a filter controller for providing an oscillator driving signal based on the plurality of range signals and the phase error signal (Fig. 9, means 80, 82, 84); an oscillator divider for providing the recovered signal based on the oscillator driving signal and at least some of the plurality of range signals (Fig. 9; Col. 6, Lines 53-Col. 7, Line 10 and Lines 22-41); wherein the phase detector, the filter controller, and the oscillator divider collectively form a phase locked loop. Koudelka is silent about a frequency detector for providing a frequency error signal based on a difference in frequencies between the input data signal and a recovered signal and a

filter controller for providing an oscillator-driving signal based on the frequency error signal. Hsu teaches a frequency detector (Fig. 2, means 12) for providing a frequency error signal based on a difference in frequencies between the input data signal and a recovered signal and a filter controller (Fig. 2, means 14) for providing an oscillator-driving signal (Fig. 2, means 18) based on the frequency error signal. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Hsu with Koudelka in order to obtain a clock and/ or data recovery circuit capable of automatically adjusting the frequency range of a voltage controlled oscillator to generate clocks in synchronization with the modulated signals.

As to claim 2, Koudelka further teaches a rate detector comprising a plurality of range sub-circuits each providing one of a plurality of range signals (Fig. 2, means 22 and 24; Col. 3, Lines 1-19; Col. 4, Lines 57-67).

As to claims 3 and 17, the range sub-circuits include an input tailoring circuit for tailoring the input data signal (means 22), a filter for filtering the tailored input data signal (Fig. 2, means 24a), and an output tailoring circuit (means 24b) for tailoring the filtered input data signal into a respective said range signal (Fig. 2, means 22 and 24; Col. Col. 3, Lines 1-19; Col. 4, Lines 57-67).

As to claims 4 and 18, Koudelka teaches the phase detector further produces a recovered data signal based on the input data signal, wherein the system is suitable for use as an clock and data recovery circuit (Col. 1, Lines 26-43).

Claims 7 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koudelka and Hsu, further in view of Shen (US 2004/0113705).

As to claims 7 and 21, Koudelka and Hsu teach all the subject matters claimed above, except for an integrator to integrate the phase error signal; a sample and hold circuit for sampling the integrated phase error signal; a frequency divider for dividing the frequency of the recovered clock signal, wherein the divided recovered clock signal gates said gated integrator and said gated sample and hold circuit; and a digital filter for filtering the sampled said phase error signal to contribute to the oscillator driving signal. Shen teaches an integrator to integrate the phase error signal; a sample and hold circuit for sampling the integrated phase error signal; a frequency divider for dividing the frequency of the recovered clock signal, wherein the divided recovered clock signal gates said gated integrator and said gated sample and hold circuit; and a digital filter for filtering the sampled said phase error signal to contribute to the oscillator driving signal (Fig. 2; Par. 15). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Shen with Koudelka and Hsu in order to drive the oscillator of the phase locked loop that provides a recovered signal.

As to claims 8 and 22, Koudelka teaches the oscillator divider includes a controllable oscillator producing an oscillating signal based on the oscillator driving signal; and at least one frequency divider for dividing the frequency of the oscillating signal; and controllably selecting one from among the oscillating signal and the divided instances of the oscillating signal to contribute to the recovered signal (Col. 2, Lines 19-47).

As to claim 9, Koudelka teaches that the controllable oscillator is a member of the set consisting of voltage-controlled oscillators, current controlled oscillators, and digitally controlled oscillators (Fig. 9, means 84).

Claims 10-14 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koudelka and Hsu, further in view of Ghiasi (US 2004/0131058).

As to claims 10 and 23, Koudelka and Hsu teach all the subject matters claimed above, except for the receiver further comprises a photo diode for converting the input data signal from an optical form to an electrical form and providing to the clock and data recovery circuit. Ghiasi teaches a receiver further comprises a photo diode for converting the input data signal from an optical form to an electrical form and providing to the next component in the receiver (Fig. 3; Par. 71). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Ghiasi with Koudelka and Hsu in order to transmit and receive signals optically, which makes data transmission faster and more efficient.

As to claims 11 and 24, Koudelka and Hsu teach all the subject matters claimed above, except for conditioning the electrical form of the input signal prior to providing it to the clock and data recovery circuit. Ghiasi teaches conditioning the electrical form of the input signal prior further processing it (Fig. 3, Par. 71). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Ghiasi with Koudelka and Hsu in order to compensate for the signal attenuation and multipath effects and preparing signal for further processing by filtering, optionally amplifying, and digitizing.

As to claim 12, Koudelka and Hsu teach all the subject matters claimed above, except for the signal conditioning circuitry includes a trans-impedance amplifier and a post amplifier. Ghiasi teaches conditioning includes a trans-impedance amplifying (Fig. 3, Par. 71). One of ordinary skill in the art would clearly recognize that conditioning includes filtering, optionally amplifying, and digitizing. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Ghiasi with Koudelka and Hsu in order to compensate for the signal attenuation and multipath effects.

As to claims 13 and 25, Koudelka and Hsu teach all the subject matters claimed above, except for converting the recovered data signal into an optical output data signal. Ghiasi teaches using a laser diode to convert the electrical transmit signal to the optical transmit signal before data transmission. Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Ghiasi with Koudelka and Hsu in order to transmit and receive signals optically (on fiber optics lines), which makes data transmission faster and more efficient.

As to claims 14 and 26, Koudelka and Hsu teach all the subject matters claimed above, except for the transceiver further includes a frequency change circuit for converting the recovered data signal based on a clock other than the recovered clock signal. One of ordinary skill in the art would clearly recognize that frequency conversion circuitries are well known in the art (i.e. RF (Radio Frequency)/IF (Intermediate Frequency) or vice versa) before data transmissions and/ or after data receptions in order to perform data transmissions more efficiently.

Claims 15 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koudelka, Hsu, and Ghiasi, further in view of Scott et al (US 2002/0130801).

As to claims 15 and 27, Koudelka, Hsu, and Ghiasi teach all the subject matters claimed above, except for the transceiver further includes a multiplexer for combining the recovered data signal and at least one other data signal. Scott teaches combining the data signal with another data signal before transmission (Pg. 12, Col. 2, Lines 15-21). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teaching of Scott with Koudelka, Hsu, and Ghiasi in order to enhance error reduction in the communications system.

Allowable Subject Matter

Claims 5-6 and 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

As to claims 5-6 and 19-20, the prior art of record fails to teach the subject matters cited in the claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Freshteh N. Aghdam whose telephone number is (571) 272-6037. The examiner can normally be reached on Monday through Friday 9:00-5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Freshteh Aghdam
November 15, 2005

KEVIN BURD
PRIMARY EXAMINER